Sub A'

1. An inrush circuit for electronic devices having high input capacitance, said inrush circuit comprising:

time delay means for eliminating false action;

means for providing a voltage ramp, operatively connected to said time delay means;

means defining an output voltage;

an operational amplifier circuit having a reference input, said operational amplifier circuit receiving said voltage ramp at said reference input and comparing a divided sample of said output voltage with the voltage ramp, said operational amplifier operating in a linear mode, whereby said output voltage approximates a multiple of the voltage ramp; and

transistor means electronically connected to said operational amplifier circuit, said transistor means operating in linear mode during capacitor charging, and subsequently reaching a full-ON

state, in order to convey full power supply capacity to a load during normal operation.

2. The inrush circuit for electronic devices in accordance with claim 1, wherein said transistor means comprises a power field effect transistor.

3. The inrush circuit for electronic devices in accordance with claim 1, wherein said output voltage approximates the voltage ramp by a gain of two.

4. The inrush circuit for electronic devices in accordance with claim 1, wherein said electronic devices comprise a point-of-sale printer.

5. The inrush circuit for electronic devices in accordance with claim 1, wherein said time delay means reaches threshold in approximately 50 ms.

5. ~~6.~~ The inrush circuit for electronic devices in accordance with claim 2, wherein said field effect transistor is operative initially in an OFF state, and subsequently becomes operative in a full-ON state.

6. ~~7.~~ The inrush circuit for electronic devices in accordance with claim ~~6~~ 5, wherein said field effect transistor is part of a linear feedback loop, and further comprising capacitive means electronically connected to said field effect transistor for ensuring that said field effect transistor is initially operative in said OFF state, said capacitive means being minimized to subsequently prevent interfering with said linear feedback loop.

7. ~~8.~~ The inrush circuit for electronic devices in accordance with claim 2, further comprising capacitive means electronically connected to said operational amplifier for preventing oscillation thereof.

9. An inrush circuit for electronic devices having high input capacitance, said inrush circuit comprising:

means for providing a voltage ramp;

means defining an output voltage;

an operational amplifier circuit having a reference input, said operational amplifier circuit receiving said voltage ramp at said reference input and comparing a divided sample of said output voltage with the voltage ramp, said operational amplifier operating in a linear mode, whereby said output voltage approximates a multiple of the voltage ramp; and

a field effect transistor electronically connected to said operational amplifier circuit, said field effect transistor operating in linear mode during capacitor charging, and subsequently reaching a full-ON state in order to convey full power supply capacity to a load during normal operation.

10. The inrush circuit for electronic devices in accordance with claim 9, wherein said output voltage approximates the voltage ramp by a gain of two.

11. The inrush circuit for electronic devices in accordance with claim 9, wherein said electronic devices comprise a point-of-sale printer.

12. The inrush circuit for electronic devices in accordance with claim 9, wherein said time delay means reaches threshold in approximately 50 ms.

13. The inrush circuit for electronic devices in accordance with claim 9, wherein said field effect transistor is operative initially in an OFF state, and subsequently becomes operative in a full-ON state.

14. The inrush circuit for electronic devices in accordance with claim 13, wherein said field effect transistor is part of a linear feedback loop, and further comprising capacitive means electronically connected to said field effect transistor for ensuring that said field effect transistor is initially operative in said OFF state, said capacitive means being minimized to subsequently prevent interfering with said linear feedback loop.

15. The inrush circuit for electronic devices in accordance with claim 9, further comprising capacitive means electronically connected to said operational amplifier, for preventing oscillation thereof.

16. The inrush circuit for electronic devices in accordance with claim 9, further comprising time delay means electronically connected to said means for providing said voltage ramp, said time delay means eliminating false action.